**IN THE CLAIMS:**

Cancel claims 1, 4 and 8.

Amend claims 2, 5 and 7 to read:

2. (Amended) A static random access memory, wherein memory cells of the static random access memory each includes:

N-type MOS transistors each having a channel-forming semiconductor region and a gate electrically connected with each other; and

P-type MOS transistors each having a channel-forming semiconductor region electrically connected with a power source,

wherein the channel-forming semiconductor regions of the P-type MOS transistors are formed of a same deep N-type well so that these channel-forming semiconductor regions are electrically connected to each other, and the channel-forming semiconductor regions of the N-type MOS transistors are formed of shallow P-type wells formed in the deep N-type well,

wherein trenches are individually provided between the channel-forming semiconductor regions of the P-type and N-type MOS transistors, said trenches being deeper than the shallow P-type wells, but shallower than the deep N-type well.

5. (Amended) A static random access memory as claimed in claim 2, comprising write circuit means that include:

MOS transistors each having a channel-forming semiconductor region and a gate electrically connected with each other.

7. (Amended) A static random access memory as claimed in claim 2, comprising read circuit means that include MOS transistors each having a channel-forming semiconductor region and a gate electrically connected with each other.